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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/897,574	07/02/2001	Kenichi Kawaguchi	10873.744US01	1221
53148	7590	03/21/2006	EXAMINER	
HAMRE, SCHUMANN, MUELLER & LARSON P.C.			HUYNH, KIM T	
P.O. BOX 2902-0902			ART UNIT	
MINNEAPOLIS, MN 55402			PAPER NUMBER	

2112

DATE MAILED: 03/21/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

<b>Office Action Summary</b>	Application No. 09/897,574	Applicant(s) KAWAGUCHI, KENICHI	
	Examiner Kim T. Huynh	Art Unit 2112	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --  
**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

#### Status

- 1) ☒ Responsive to communication(s) filed on 10 January 2006.  
2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.  
3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

#### Disposition of Claims

- 4) ☒ Claim(s) 1-14 is/are pending in the application.  
4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.  
5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.  
6) ☒ Claim(s) 1-14 is/are rejected.  
7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.  
8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

#### Application Papers

- 9) ☐ The specification is objected to by the Examiner.  
10) ☒ The drawing(s) filed on 07 February 2001 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).  
11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

#### Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).  
a) ☐ All b) ☐ Some \* c) ☐ None of:  
1. ☐ Certified copies of the priority documents have been received.  
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.  
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).  
\* See the attached detailed Office action for a list of the certified copies not received.

#### Attachment(s)

- |  |   |
|--|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892)   | 4) <input type="checkbox"/> Interview Summary (PTO-413)<br>Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)                                   | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152)             |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)<br>Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____  |

## DETAILED ACTION

### ***Claim Rejections - 35 USC § 102***

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1-14 are rejected under 35 U.S.C. 102(e) as being anticipated by West (US Patent 6,195,730)

As per claims 1, 6 West discloses a data transfer apparatus comprising:

- An associative memory(fig.1, 46 ie IOP local memory) connected between a system bus(fig.1, 28 ie system bus) and a local bus(fig.1, 36 ie IOP expansion bus); and (col.4, lines 38-60)
- A controller(fig.1, 44 ie IOP microprocessor) for controlling data input/output of the associative memory; (col.3, lines 1-16)
- Wherein the controller of the data transfer apparatus, the data transfer apparatus being a first device, fetches an address and data that are transferred between a second device and a third device (fig.1, 26, ie IOP) that are connected only on the system bus so as to duplicate and store

them in the associative memory, (col.3, lines 35-45), (also see col.5, line 11-col.6, line 22, ie cache memory 62)

- When a fourth device (fig.1, 22 ie storage device) on local bus generates a read cycle to read data from a read address associated with one of the second and third devices on the system bus and the read address is contained in the address stored in the associative memory, the controller reads out corresponding data from the associative memory so as to transfer it to the local bus. (col.3, lines 1-46 ie any storage devices is required for the data transfer, the request is mapped in the cache memory to the storage devices capable of servicing the request and transferring via IOP expansion bus(local bus)), (also see col.5, line 11-col.6, line 22, ie cache memory 62)

As per claims 2, 7, West discloses wherein if it is detected that a write cycle of writing a data from one of the second or third devices to another device of the second or third devices is generated on the system bus, the controller fetches the address and the data that are transferred between the second and third devices so as to duplicate and store them in the associative memory. (col.3, lines 1-45)

As per claims 3,8, West discloses wherein the controller monitors a data output enable signal line of at least one device controller on the system bus and, when the data output enable signal line is asserted, fetches the address and the data

that are transferred on the system bus so as to duplicate and store them in the associative memory. (col.3, lines 1-45)

As per claims 4,9, West discloses wherein the controller monitors a data output strobe signal line of at least one device controller on the system bus and, when the data output strobe signal line is asserted, fetches the address and the data that are transferred on the system bus so as to duplicate and store them in the associative memory. (col. 3, lines 1-45)

As per claims 5, 10, West discloses wherein when the address from which the data is transferred indicated by the data transfer request accepted from the local bus is not contained in the address stored in the associative memory, the controller stores a data effective information indicating the address in which a transfer operation has not been completed in response to the data transfer request in a second associative memory, fetches the address and the data that are transferred between the devices on the system bus and, if the fetched address is the address indicated by the data effective information, transfers it to the local bus as data corresponding to the data transfer request. (col.7, line 66- col.9, line 34 ie controller maps the data transfer request to cache device (correlates mapping table) and determine whether or not the requested data is currently contained within cache memory)

As per claim 11, West discloses a data transfer apparatus comprising:

- An associative memory (fig.1, 46 ie IOP local memory) connected between a system bus(fig.1, 28 ie system bus) and a local bus fig.1, 36 ie IOP expansion bus); and (col.4, lines 38-60)
- A controller for controlling data input/output of the associative memory;
- A controller(fig.1, 44 ie IOP microprocessor) for controlling data input/output of the associative memory; (col.3, lines 1-16)
- Wherein the controller of the data transfer apparatus, the data transfer apparatus being a first device, fetches an address and data that are transferred between devices (fig.1, 26, ie IOP) that are connected only on the system bus so as to duplicate and store them in the associative memory, (col.3, lines 35-45), (also see col.5, line 11-col.6, line 22, ie cache memory 62)
- Fetches an address and a data that are transferred between devices on the local bus so as to duplicate and store them in the associative memory, (col.3, lines 35-45), (also see col.5, line 11-col.6, line 22, ie cache memory 62)
- When a fourth device(fig.1, 22 storage device) on the local generates a read cycle to read data from a read address associated with one of the second and third devices on the system bus and the read address is contained in the address stored in the associative memory, the controller reads out a corresponding data from the associative memory so as to

transfer it to the local, accepts a data transfer request from the system bus and, when an address from which the data is transferred indicated by the data transfer request it contained in the address stored in the associative memory, reads out corresponding data from the associative memory so as to transfer it to the system bus. (col.3, lines 35-45), (also see col.5, line 11-col.6, line 22, ie cache memory 62)

As per claim 12, West discloses a data transfer method for controlling data input/output between a system bus and a local bus the method comprising:

- A buffering operation of a data transfer apparatus comprising a first device, of fetching an address and data that are transferred between a second device and a third devices that are connected only on the system bus so as to duplicate and store them; and (col.3, lines 35-45), (also see col.5, line 11-col.6, line 22, ie cache memory 62)
- An operation of accepting a data transfer request from the local bus when a device on the local bus generates a read cycle to read data from a read address associated with one of the devices on the system bus and the read address is contained in the address stored in the buffering operation; and (col.3, lines 35-45), (also see col.5, line 11-col.6, line 22, ie cache memory 62)
- Reading out corresponding data so as to transfer it to the local bus. (col.3, lines 1-46 ie any storage devices is required for the data

transfer, the request is mapped in the cache memory to the storage devices capable of servicing the request and transferring via IOP expansion bus(local bus)), (also see col.5, line 11-col.6, line 22, ie cache memory 62)

As per claim 13, West discloses a data transfer method for controlling data input/output between a system bus and a local bus, the method comprising:

- A buffering operation of a data transfer apparatus comprising a first device, of fetching an address and data that are transferred between a second and a third devices that are connected only on the local bus so as to duplicate and store them in an associative memory connected between the system bus and the local bus; and (col.3, lines 35-45), (also see col.5, line 11-col.6, line 22, ie cache memory 62)
- An operation of accepting a data transfer request from the system bus and, when a fourth device on the system bus generates a read cycle to read data from a read address associated with the second or third devices on the local bus and the read address is contained in the address stored in the buffering operation; and (col.3, lines 35-45), (also see col.5, line 11-col.6, line 22, ie cache memory 62)
- Reading out corresponding data so as to transfer it to the system bus.  
(col.3, lines 35-45), (also see col.5, line 11-col.6, line 22, ie cache memory 62)



As per claim 14, West discloses a data transfer method for controlling data input/output between a system bus and a local bus, comprising:

- A first buffering operation of a data transfer apparatus comprising a first device, of fetching an address and data that are transferred between a second device and a third devices (fig.1, 26 ie IOP) that are connected only on the system bus(fig.1, 28 ie system bus) so as to duplicate and store them; (col.3, lines 35-45), (also see col.5, line 11-col.6, line 22, ie cache memory 62)
- A second buffering operation of fetching an address and data that are transferred between a fourth device and a fifth devices (fig.1, 22 ie storage devices) which are connected only on the local bus(fig.1, 36 ie IOP expansion bus) so as to duplicate and store them; (col.3, lines 35-45), (also see col.5, line 11-col.6, line 22, ie cache memory 62)
- A first data transfer operation of accepting a data transfer request from the local bus and, when the fourth or fifth devices on the local bus generates a read cycle to read data from a read address associated with the second or third devices on the system bus and the read address is contained in the address stored in the first buffering operation, reading out corresponding data so as to transfer it to the local bus; and (col.3, lines 35-45), (also see col.5, line 11-col.6, line 22, ie cache memory 62)

- A second data transfer operation of accepting a data transfer request from the system bus when the second or third devices on the system bus generates a read cycle to read data from a read address associated with the fourth or fifth devices on the local bus and the read address is contained in the address stored in the second buffering operation, reading out corresponding data so as to transfer it to the system bus. (col.3, lines 35-45), (also see col.5, line 11-col.6, line 22, ie cache memory 62)

***Response to Amendment***

3. Applicant's amendment filed on 1/10/06 have been fully considered but does not place the application in condition for allowance.

a. In response to applicant's argument that West does not disclose or suggest a data transfer apparatus or method including a controller that fetches an address and data that are transferred between a second device and a third device that are connected only on the system bus so as to duplicate and store them in an associative memory. Examiner respectfully disagrees. As West notes at col.3, lines 1-21, discloses the control logic receives(fetch) a data transfer request from host. The request is mapped (duplicated) to a cache device, the cache device has associated data maintained in the cache memory. If any storage devices(different devices) is required for the data transfer, the request is mapped to the device. This is equivalent to applicant's amended claims. Thus, the prior art teaches the invention as claimed and the amended claims do not distinguish over the prior art as applied.

b. In response to applicant's argument that West does not disclose a data transfer apparatus or method including a fourth device on the local bus that generates a read cycle to read data from a read address associated with the second or third devices on the system bus, where when the read address corresponds to the address stored in the associative memory, the controller transfers the corresponding data from the associative memory to the local bus. Examiner respectfully disagrees. As West notes at col.3, lines 1-45, ie If any storage devices(different devices) is required for the data transfer, the request is mapped to the device. A location in cache memory is mapped from request. In one embodiment, the IOP is connected to a sending storage device and a receiving storage device. The control logic read data in a first data format from sending storage device and buffering data in a cache memory and then write data in a second data format to the receiving storage device. Thus, the prior art teaches the invention as claimed and the amended claims do not distinguish over the prior art as applied.

### ***Conclusion***

**4. THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the

shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

5. *Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kim Huynh whose telephone number is (571)272-3635 or via e-mail addressed to [kim.huynh3@uspto.gov]. The examiner can normally be reached on M-F 9:00AM- 6:00PM. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Rehana Perveen can be reached at (571)272-3676 or via e-mail addressed to [rehana.perveen@uspto.gov].*

*The fax phone numbers for the organization where this application or proceeding is assigned are (571)273-8300 for regular communications and After Final communications. Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (571)272-2100.*

Kim Huynh

March 14, 2006

  
REHANA PERVEEN  
SUPERVISORY PATENT EXAMINER  
3/16/06